An FPGA-based Hardware-Efficient Fault-Tolerant Astrocyte-Neuron Network

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***Abstract*—The human brain is structured with the capacity to repair itself. This plasticity of the brain has motivated researchers to develop systems which have similar capabilities of fault tolerance and self-repair. Recent research findings have proven that interactions between astrocytes and neurons can actuate brain-like self-repair in a bidirectionally coupled astrocyte-neuron system. This paper presents a hardware realization of the bio-inspired self-repair architecture on an FPGA. We also introduce a reduced architecture for an FPGA-based hardware-efficient fault-tolerant system using the principle of retrograde signaling in an astrocyte-neuron network by simplifying the calcium dynamics within the astrocyte. The hardware optimized implementation shows more than a 90% decrease in hardware utilization and proves an efficient implementation for a large-scale astrocyte-neuron network. Average spike rate of 0.027 spikes per clock cycle were observed for both the proposed models of astrocytes in the case of 100% partial fault.**

I. Introduction

Electronic systems are increasingly used in safety critical applications that demand low failure rates and fault tolerance. Fault tolerance has always been a standard feature of electronic systems targeted for long-life applications. Novel approaches to fault tolerance can be achieved by drawing inspiration from natural processes. Bio-inspired systems derive motivation from biological processes in the development of massively parallel computationally efficient systems. The human brain has remarkable computational capabilities, which can outperform standard computer systems in many real-world tasks. The brain is exceptional in its ability to self-repair, for example following stroke or injury. A number of researches have demonstrated the potential of bio-inspired systems to achieve fault tolerance similar to a human brain [1]–[7]. It has been recently found that retrograde signaling via astrocytes has the capability to facilitate self-repair [8]. Astrocytes are star-shaped glial cells found in Central Nervous System (CNS) and Peripheral Nervous System (PNS) that enclose multiple synapses connected to a neuron. Astrocytes have the capacity to communicate in a feedback mode with the neurons, thereby establishing a bidirectional communication with the neurons forming a tripartite synapse that can self regulate neuronal activity [9].

In biological systems, independent units perform computation in parallel. For real world applications, this parallelism can be exploited to perform tasks orders of magnitude faster than in software. FPGAs are preferred to GPUs for artificial neural networks applications [10], [11] due to their reconfigurability. Using FPGAs to implement artificial neural networks are an excellent choice because they combine computing capability, logic resources and memory capacity in a single device. In this work we employ FPGAs to implement the astrocyte-neuron based self-repairing unit. Designing any system to tolerate faults first requires the selection of a fault model, a set of possible failure scenarios along with an understanding of the depth and impact of each scenario. There can be various kinds of faults in a system when implemented in hardware including permanent faults (eg. ageing faults, manufacturing defects, single event upsets) and temporary fault (eg. power supply fluctuations, radiations). In this work we describe faults as a condition which results in a silent or near silent neuron caused by low transmission probability (PR) of a synapse, and repair is defined as the ability of the system to restore firing rates through an increase of PR. Our results demonstrate the ability of an FPGA-based implementation to exhibit self-repair under this fault condition.

The architectures proposed in this paper reduce the resource requirements for the astrocyte-neuron self-repair unit by:

1) **Model-I of astrocyte**: We have developed an improvised architecture for the self-repair unit by using approximation techniques for calcium dynamics of the astrocyte.
2) **Model-II of astrocyte**: We have developed a compact design methodology for implementing self-repair in the astrocyte-neuron network by eliminating the complex processes occurring within the astrocyte. The developed architecture is more than 90% resource efficient compared to [12].

The rest of the paper is organized as follows: Section II discusses the basics of the astrocyte-neural network model, followed by the proposed hardware implementation of the astrocyte-neuron self-repairing unit emphasizing a hardware-efficient astrocyte implementation in Section III. In Section IV, a reduced model of the self-repairing astrocyte-neuron network is presented. Section V presents our experimental results , and conclusions are drawn in Section VI.

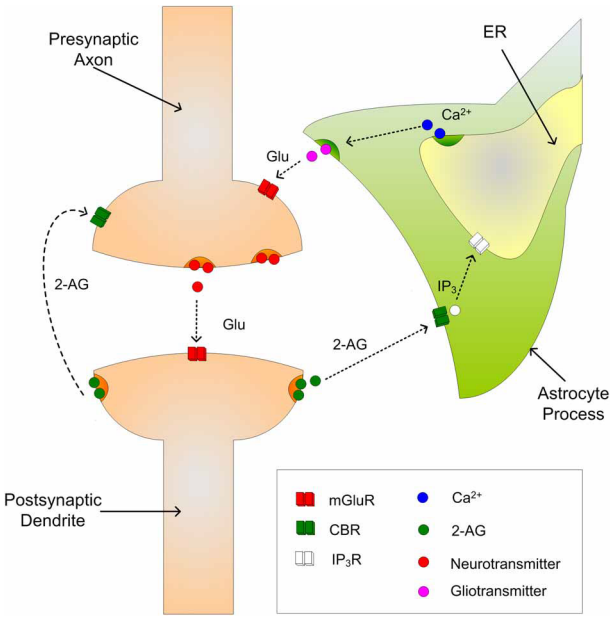

Fig. 1: **The tripartite synapse showing indirect and direct signaling of 2-AG, figure from [8].**

II. Astrocyte-Neural network Model

The structure and working of the astrocyte-neuron self-repairing unit can be summarized as follows, in conjunction with Fig. 1.

1) We consider a tripartite synapse consisting of a pre-synaptic neuron, a post-synaptic neuron, and an astrocyte. If a post-synaptic neuron is sufficiently depolarized due to an arrival of action potential (AP) from a pre-synaptic neuron, a retrograde messenger (endocannabinoid) is released by the post-synaptic neuron.
2) The endocannabinoid retrograde messenger travels back from the post-synaptic neuron to pre-synaptic neuron through two different paths. One method is by directly binding to the corresponding cannabinoid receptors (direct signaling) and the second is via an astrocyte leading to a series of chemical reactions occurring at the astrocyte end (indirect signaling). The direct signaling leads to decrease in transmission probability of the synapse and is termed as Depolarization-induced Suppression Excitation (DSE). The indirect signaling results in an increase of synaptic transmission and is termed eSP. The eSP signaling is due to the occurrence of a series of chemical reactions in the astrocyte and neuron including the release of 2-arachidonyl glycerol (2-AG), inositol trisphosphate ($IP3$), calcium (Ca^{2+}), and glutamate (Glu).
3) The direct signaling pathway is local in nature and only binds to a few neurons, whereas the indirect signaling pathway is global in nature and can reach distant synapses via the astrocyte network.
4) Due to the action of DSE and eSP, the transmission probability of synapse is reduced by 50% in the equilibrium state. This is because DSE overpowers eSP.
5) When individual synapses associated with a neuron fail, (a condition of low transmission probability), the direct signaling decreases, but the indirect signaling via astrocytes increases the transmission probability, thereby repairing the fault. For more details, see [8].

The transmission probability (PR) of any synapse modulated by the effects of DSE and eSP is given by:

$$PR(t) = PR(t_0)(1 + \frac{DSE + eSP}{100}) \tag{1}$$

where $PR(t_0)$ is the initial PR of the synapse. The sequence of events occurring at a tripartite synapse are briefly explained as follows: when a post-synaptic neuron fires, 2-AG is released. This is describe by the following relation:

$$\frac{d(AG)}{dt} = \frac{-AG}{\tau_{AG}} + \gamma_{AG}\delta(t - t_{sp}) \tag{2}$$

where AG is the amount of 2-AG released. τ_{AG} and γ_{AG} is the decay rate and the production rate of 2-AG respectively. t_{sp} is the time at which the post-synaptic neuron fires. The 2-AG released from the neuron give rise to a direct signaling at the tripartite synapse, leading to a reduction in PR. The relation between the amount of 2-AG released and the DSE is modeled using a linear equation as follows:

$$DSE = AG \times K_{AG} \tag{3}$$

where K_{AG} is a scaling factor used to balance equation (1).

In addition to direct signaling, The 2-AG released from the neurons associated with the astrocyte can also bind to the corresponding receptors ($CB1Rs$) on the astrocyte. This leads to the production of IP_3 within the astrocyte.

$$\frac{d(IP_3)}{dt} = \frac{IP_{3_{base}} - IP_3}{\tau_{IP_3}} + \gamma_{IP_3}\sum_{i=1}^{q} AG \tag{4}$$

where IP_3 is the amount of IP_3 released within the astrocyte's cytoplasm in response to 2-AG. $IP_{3_{base}}$ is the baseline of IP_3 when the astrocyte is in steady state. τ_{IP_3} and γ_{IP_3} is the decay rate and the production rate of IP_3 respectively. q is the number of neurons associated with an astrocyte.

In contrast to Wade et.al [8], we are using a parallel approach by considering the total 2-AG arriving at the astrocyte surface.

In response to alleviated IP_3, calcium builds up within the astrocyte. This is given by the following equation.

$$\frac{d(Ca^{2+})}{dt} = J_{chan}(Ca^{2+}, h, IP_3) + J_{leak}(Ca^{2+}) - J_{pump}(Ca^{2+}) \tag{5}$$

where J_{chan} is the calcium release dependent on IP_3 and Ca^{2+}, J_{leak} models the leakage of Ca^{2+} out of the Endoplasmic Reticulum (ER) and J_{pump} is the amount of Ca^{2+} pumped into the ER. More details of astrocyte calcium dynamics are given in [13]. When the amount of calcium crosses certain threshold value, calcium spikes are formed, which in turn stimulate the release of glutamate (Glu). The amount of glutamate produced is given by:

$$\frac{d(Glu)}{dt} = \frac{-Glu}{\tau_{Glu}} + \gamma_{Glu}\delta(t - t_{ca}) \tag{6}$$

where Glu is the amount of glutamate discharged. τ_{Glu} and γ_{Glu} is the decay rate and the production rate of glutamate

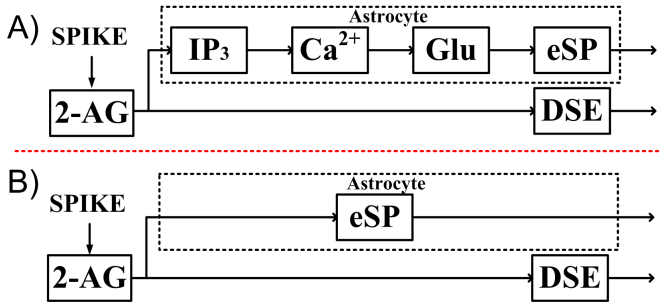

Fig. 2: **Block diagram representing chain of biological processes involved in eSP and DSE production. (A)** Model-I **(B)** Simplified Model-II of an astrocyte

respectively. t_{ca} is the time at which the calcium spikes. The glutamate released from the astrocyte binds to the corresponding receptors (group 1 $mGluRs$) on the pre-synaptic neuron. This accelerates indirect signaling at the tripartite synapse leading to enhancement of PR. The indirect signaling is modeled using the following equation:

$$\tau_{eSP}.\frac{d(eSP)}{dt} = -eSP + m_{eSP}Glu(t) \tag{7}$$

where τ_{eSP} is the decay rate eSP and m_{eSP} is a weighting constant used to balance equation (1). By the action of DSE and eSP the PR depicted in equation (1) reduces to $\sim 50\%$. We use a *Leaky Integrate and Fire* (LIF) [14] model for representing the neurons in the network. This is shown below:

$$\tau_{mem}\frac{dv}{dt} = -v(t) + R_{mem}\sum_{i=1}^{m} {I_{syn}}^{i}(t) \tag{8}$$

where τ_{mem}, R_{mem} and v are the time constant, membrane resistance and membrane potential respectively. m represents the number of synapses associated with a neuron. On reaching the threshold voltage, the membrane potential is brought back and held at 0V for $2ms$, there by implementing a refractory period.

A probabilistic model is used for representing the synapse and is given by:

$${I_{syn}}^{i}(t) = \begin{cases} I_{inj}, rand \leq PR, \\ 0, rand > PR \end{cases} \tag{9}$$

A *Linear Feedback Shift Register* (LFSR) is used to generate a random number ($rand$). A fixed amount of current I_{inj} is injected into the synapse if the random number is less than or equal to the PR. The whole process involved is depicted in a block diagram shown in Fig. 2A.

III. FPGA-BASED ASTROCYTE NEURON NETWORK (MODEL-I)

The basic unit (Model-I) of a self-repairing astrocyte-neuron network is shown in Fig. 3. The architecture consists of two neurons (N1 and N2) and an astrocyte (A) shared between these two neurons. Each neuron is associated with a set of synapses (10 in our experiments). The synapses receive input spikes from other neurons. Any healthy synapse is related to an initial PR of 0.5. For testing the basic unit, we used

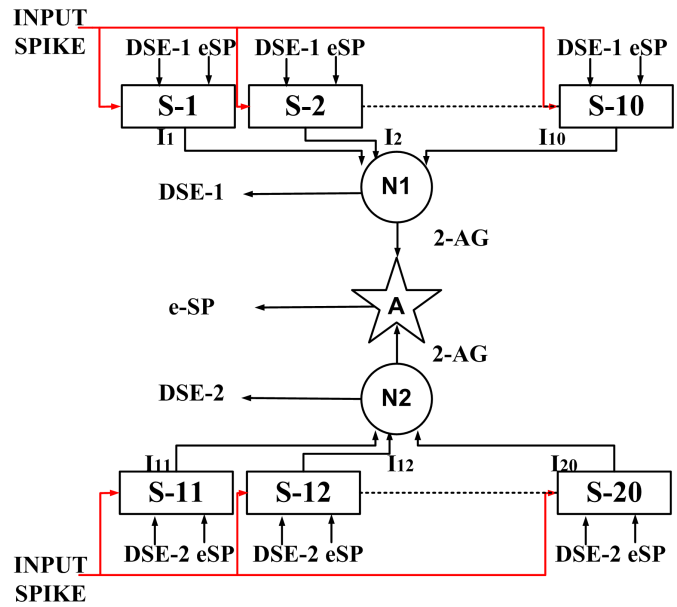

Fig. 3: **Basic unit for self repair mediated by an astrocyte** Two neurons $N1$ and $N2$, each receives 10 synaptic inputs ($S-1$ to $S-10$ and $S-11$ to $S-20$). A represents the astrocyte connected with $N1$ and $N2$. The signals $DSE-1$ and $DSE-2$ are local to synapses connected to $N1$ and $N2$ respectively, whereas eSP is a global signal associated with all synapses connected to A.

Poissons spike trains, which on an average, produce one spike per 4 clock cycles. In addition to the spike inputs, the synapses receive the direct signaling from the associated neuron and the indirect signaling from the associated astrocyte. The synapse processes these signals and makes a decision on the current to be injected onto the neuron. This is based on equations 1 and 9. In response to the total current injected, the neuron produces 2-AG leading to direct signaling. Also, an indirect signaling pathway is initiated via the astrocyte. The astrocyte processes the total 2-AG accumulated on its surface leading to indirect signaling through a set of complex processes represented in equation (4)–(7). Note that, the eSP signal generated from astrocyte A is common to all synapses associated with neurons connected to it. The two signals (DSE and eSP) are balanced at the synapses so that the PR falls to 50% of the initial value once the system operates fully. The condition of a fault in a synapse is modeled by lowering the initial PR value to 0.

When a synapse fails, the current injected by it falls to $zero$ as per equation 9. This lowers the 2-AG production and hence DSE falls, but the eSP signal exists in the system. Consider a case when all the synapses associated with $N2$ fail. Here, due to the presence of indirect pathway through neuron $N1$ and the astrocyte A, the PR of the synapses associated with $N2$ is raised leading to an increase in spiking activity of $N2$ after the fault.

The calcium dynamics for implementing the biological processes within the astrocyte requires complex multiplications and divisions as evident from [8] and [13]. Also, the biological parameters are precise in nature and require floating-point

arithmetic for reproducing exact functionalities. A division implemented in a *Xilinx Intellectual Property* (IP) core requires a latency of the order $M+F$ (M is the width of dividend, and F is the width of fractional reminder) clock cycles [15]. This implies that a chain of biological processes, at the astrocyte end, requires a higher latency (without pipelining). Additionally, implementing the floating point divisions involved in calcium dynamics of the astrocyte consumes an enormous amount of hardware resources. Hence when modeling an astrocyte process, the main operation to be approximated is division. In this work we approximate divisions involved in astrocyte calcium dynamics.

All the division operations involved in the calcium dynamics are approximated by sampling the constituent curves at regular intervals. The sampled values are stored in the FPGA for future use. We use a sampling interval of 0.06 μM for calcium and IP_3. If greater accuracy is required, the sampling rate may be increased. One aspect of our model is that it operates at an accelerated biological time scale similar to that in [16]. Various parameters used in this model are listed in Table I.

IV. Reduced Architecture for Bio-inspired Self Repair (Model-II)

It has been found that astrocytes can encapsulate$\sim 10^5$ synapses and connect to multiple neighboring neurons [17], [18]. The biggest problem we face with the hardware realization of the classical model of astrocyte (Wade et al.'s astrocyte model), incorporating the chain of complex chemical reactions, is the increased hardware footprint. We are interested in the accuracy and scalability of the neural networks. There is between 10 and 50 times more glia than neurons in the central nervous system of vertebrates [19] and particularly, astrocytes outnumber neurons by over fivefold [20]. To mimic brain-like functionality, the size of each astrocyte plays an important role. One of the main threats to the scalability of a network is the increased hardware utilization incurred in implementing the astrocyte. Considering scalability as an important metric it is time to revisit the complex self-repairing astrocyte-neuron structure and reduce its complexity. Hence the motivation behind the work presented in this paper is to simplify the existing architecture in terms of hardware, while retaining key features of direct negative feedback and the indirect positive feedback.

First, we simplify astrocyte equations (4)–(7) based on our observations, that imply that the two features which underpin the spiking activity of a neuron are the balance between the direct and indirect signaling. In the reduced model, we simplify the astrocyte model by eliminating some activities within the astrocyte to reduce the complexity in building up a self-repair unit. The modified block diagram is presented in Fig. 2B.

Similar to the self-repair architecture described in Section III, when a neuron is sufficiently depolarized, it produces 2-AG which leads to direct signaling. Equation (2) holds true for this model also. Equations (4)-(7) are merged to a single equation given by:

$$\tau_{eSP}\frac{d(eSP_u)}{dt} = -eSP_u + m_{eSP}\sum_{i=1}^{q} AG \qquad (10)$$

where τ_{eSP} is the decay rate eSP and m_{eSP} is a weighting constants. q is the number of neurons associated with an astrocyte.

$$eSP = K_2 \times eSP_u \qquad (11)$$

where K_2 is a scaling constant used to balance equation (1). By the action of DSE and eSP the PR depicted in equation (1) reduces to $\sim 50\%$. Various parameters used in this reduced model (Model-II) are listed in Table I.

V. Experimental Results

The hardware architectures shown in Fig. 2, for both astrocyte Model-I and Model-II, were designed using Verilog HDL. The designs were synthesized and implemented using *Xilinx ISE 14.7* CAD software for the *Xilinx Artix-7* target platform working at 100MHz clock frequency, and were simulated using *Xilinx Isim*. Power estimation of the circuits was carried out using *Xilinx XPower Analyzer* and delay estimation using *Xilinx Timing Analyzer*. *Xilinx Chipscope Pro* was used for monitoring the activities of the system in the real hardware. We use *Euler method* of integration with a fixed step size of $\Delta t = 2^{-10}$. To represent floating point numbers we use a 32-bit representation were the first 16-bits represent the integer part, and the remaining 16-bits represents the decimal part. For example $I_{inj} = 415.625mA = 32'h019F_A000$.

A. Implementation without Fault

In the first test case, all synapses had an initial PR ($PR(t_0)$) of 0.5, i.e. no fault condition (fault rate=0%). The synapses associated with Neuron $N1$ and $N2$ receives both DSE and eSP. Based on the input spike train and the PR, a decision is made on the amount of current injected to the neurons. When the input current is large enough to build up the membrane potential to a value higher than the threshold, the neuron outputs a spike. Fig. 4(A) shows the corresponding rise in negative DSE signal for $N2$ (similar behavior is observed for DSE of $N1$). Fig. 4(B) shows the eSP signal which is common to both $N1$ and $N2$. The PR of synapses associated with $N2$ is shown in Fig. 4(C). Fig. 4(D) shows the average spiking activity of the neuron $N2$. PR and spiking activity for $N1$ is similar to that for $N2$ (not shown in figure). For determining the spiking activity, we use a window of size 128 clock cycles. In our model, the DSE and eSP signals achieve steady states within one millisecond. This emphasis that the hardware model developed reaches a steady state value in less than a millisecond thereby resulting in a stable PR faster than the simulation model presented in [8], which achieves a steady state value after $100s$. Hence the hardware implementation of the model presented in this paper has a better efficiency. This is achieved by using an accelerated biological time scale in our hardware implementation.

B. Implementation with Fault

We implement a "faulty" synapse by lowering its initial PR to a value lower than 0.5. For instance, the initial PR of 80% of synapses associated with neuron $N2$ are intentionally lowered to 0 from 0.5 at $1000\mu s$, i.e., 8 out of 10 synapses of neuron $N2$ are injected with a fault. Fig. 5(A)(model-I) shows that PR of synapse-1, a faulty synapse, which initially undergoes a depression (at $1000\mu s$), but tries to increase

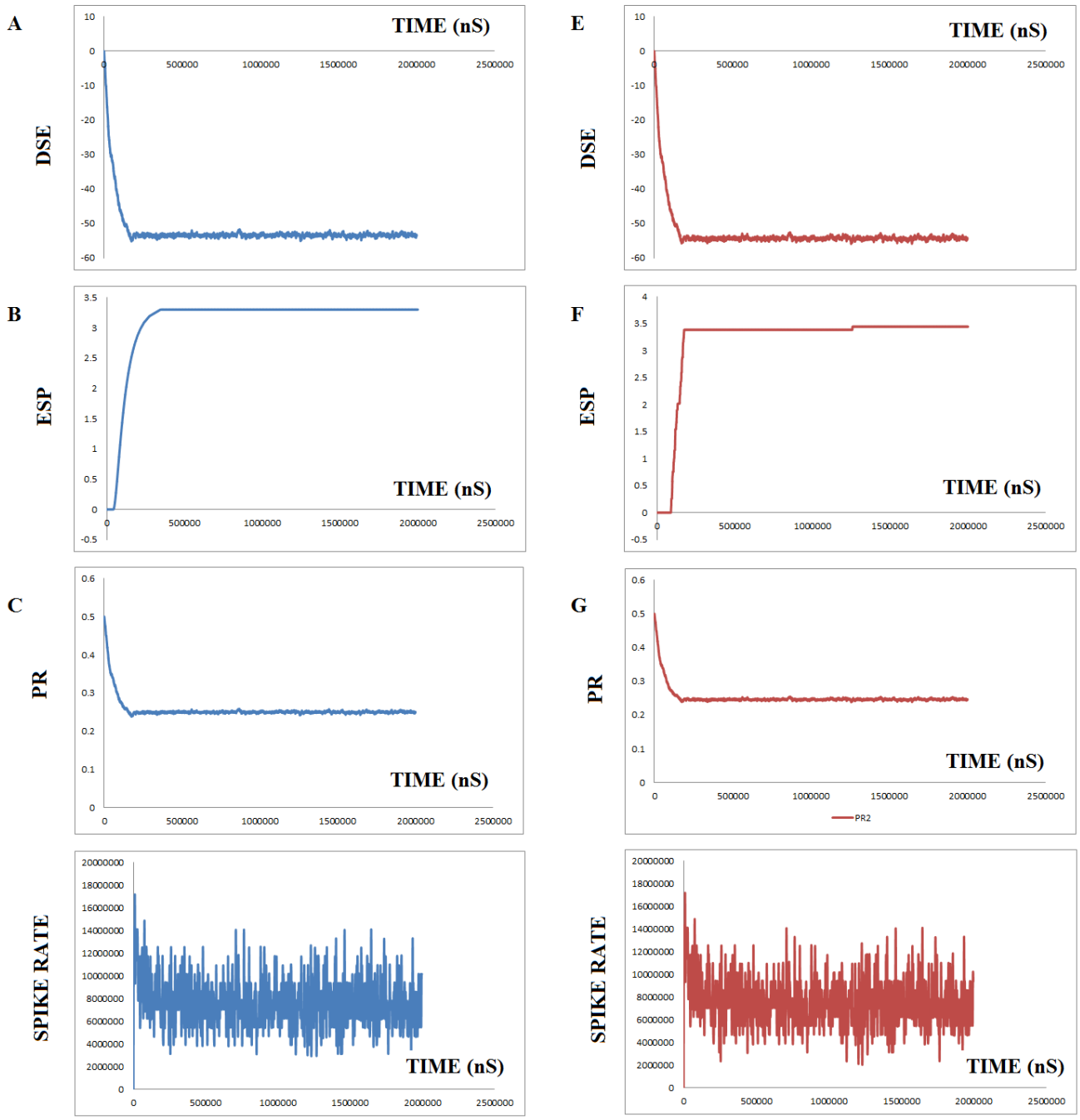

Fig. 4: **Astrocyte-Neuron self repairing unit with no fault (A–D)** for model-I (left) and **(E–H)** for model-II (right) of astrocyte. **(A, E)** DSE function of $N2$ (similar behavior is observed for DSE of $N1$). **(B, F)** eSP signal of both $N1$ and $N2$. **(C, G)** The probability of synapses connected to $N1$ and $N2$. **(D, H)** Firing rates of $N2$ (similar behavior is observed for firing rate of $N1$).

thereafter due to the repair. This behavior holds true for other faulty synapses also. The PR of healthy synapses of $N2$ increases to recoup the network faults as shown in Fig. 5(B). The PR of all synapses of neuron $N1$ remains unaffected as plotted in Fig. 5(C). Fig. 5(D) demonstrates the increase in spike frequency of $N2$ after the repair. Note: at $1000\mu s$ a dip in frequency is observed, and thereafter due to the self-repairing capability the spike rate increases. Fig. 5(E–H) shows same results for the reduced model-II.

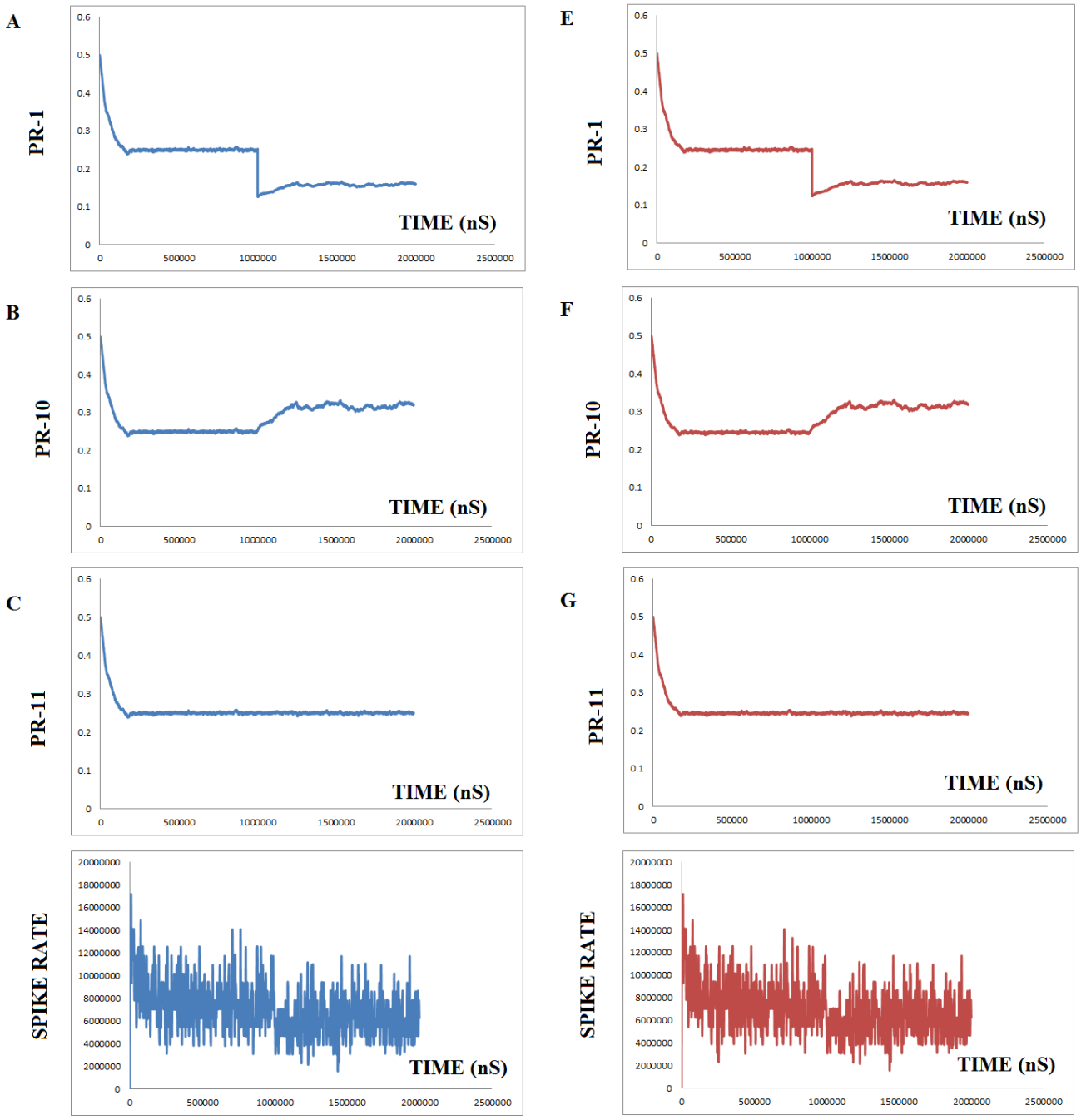

Fig. 5: PR **values of synapses and the firing rate of neuron** $N2$ **for a fault of** 80% **in synapses connected to** $N2$ **(A–D)** for model-I (left) and **(E–H)** for model-II (right) of astrocyte. **(A, E)** PR values of a faulty synapse of $N2$ (similar behavior is observed for all faulty synapses of $N2$). **(B, F)** PR values of a non-faulty synapse of $N2$ (similar behavior is observed for all non-faulty synapses of $N2$). **(C, G)** PR values of a synapse of $N1$ (similar behavior is observed for all synapses of $N1$). **(D, H)** Firing rates of $N2$ showing a rate falling after $1000\mu s$ and increasing there after due to the repair initiated by the astrocyte.

C. Implementation without an Astrocyte

The system is tested in the presence and absence of an astrocyte. Fig. 6 plots the spiking activity of neuron N2 in the self-repairing unit neuron implemented on the FPGA. This is captured using *Xilinx ChipScope* CAD software. After some time, we induced a fault of 100% in neuron $N2$. The model containing an astrocyte induced with partial fault Fig. 6(A) shows spiking activity due to the repair initiated in

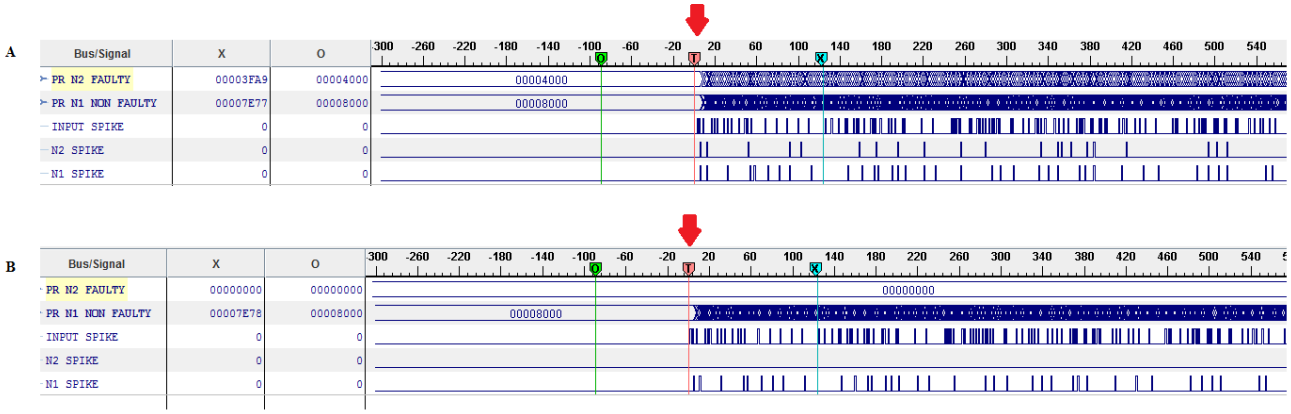

Fig. 6: **Chipscope results on real hardware (Nexys-4 Artix-7 FPGA board):** Fault of 100% is induced on synapses connected to $N2$ at the trigger point T **(A)** Partial fault ($PR(t_0) = 0.25$)**(B)** Catastrophic fault ($PR(t_0) = 0.0$). The PR values of faulty synapse lowers to $zero$ in the presence of catastrophic faul twhereas has a moderate value in the presence of partial fault. Also the spikes produced by $N2$ ceases in the case of catastrophic fault, whereas has a moderate value in the presence of partial fault.

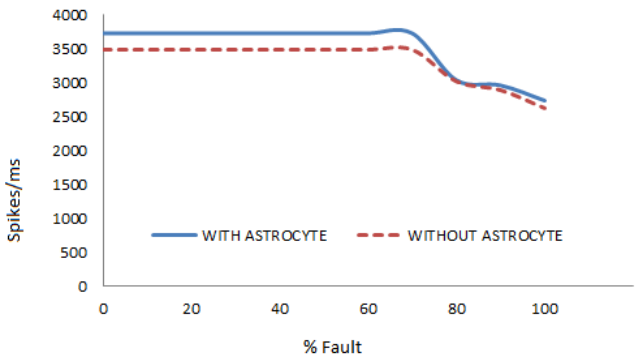

Fig. 7: **Average firing rate of self repairing unit an astrocyte (red) and without an astrocyte (blue)**. It can be seen that the spike rate is higher in all cases in the presence of astrocyte.

the device. In the presence of an astrocyte with a catastrophic fault 6(B), the neuron $N2$ remains stagnant without producing any spikes. Also the PR associated with the faulty synapse is 0 in the presence of catastrophic fault, but has a moderate value (0.023 spikes per clock cycle) in the presence of partial fault. Similar behavior is observed for the reduced model-II also (not shown). Faults of 70% 80%, 90% and 100% were introduced to neuron $N2$ of the system (Fig. 7) (model-I). It is evident that spiking activity is higher for the architecture with an astrocyte, thereby demonstrating the repair capability. It can be seen that the firing rate is higher in the presence of an astrocyte in all cases where faults are introduced. This figure holds true for both the models.

D. Power Dissipation, Delay and Hardware Resource Overheads

Estimated power dissipation and delay of the overall architecture consisting of astrocytes of Model-I and Model-II

TABLE I: **Parameters used in self-repairing astrocyte-neuron network**

Parameters*	Wade et.al [8]	Model-I	Model-II
V_{th}	$9mV$	$1mV$	$1mV$
R_m	$1.2G\Omega$	1.21Ω	1.21Ω
τ_{mem}	$60ms$	$60ms$	$60ms$
I_{inj}	$6650pA$	$415.6251mA$	$415.6251mA$
γ_{AG}	$0.8\mu M$	$0.9999\mu M$	$0.9999\mu M$
τ_{AG}	$10s$	$10s$	$10s$
γ_{IP_3}	$0.5\mu M$	$0.5\mu M$	$---$
τ_{IP_3G}	$7s$	$7s$	$---$
Ca_{th}	0.3	0.697	$---$
γ_{Glu}	$10\mu M$	$0.625\mu M$	$---$
τ_{Glu}	$100ms$	$1.61s$	$---$
τ_{eSP}	$40s$	$7s$	$7s$
m_{eSP}	55×10^3	3.5	0.21875
*Model-I uses same set of parameters for implementing calcium dynamics as in [8]			

TABLE II: **Power dissipation and delay overheads**

Model-I		Model-II	
Power (W)	**Delay (ns)**	**Power (W)**	**Delay (ns)**
0.339	37.343	0.173	15.792

are shown in Table II. Table III reports the hardware resource footprint of both the models in comparison with the direct hardware implementation of [8]. As evident from these tables, the proposed architectures can be implemented with reduced hardware overhead and the power dissipation and delay are also less. Additionally, it is clear that Model-II is better for

TABLE III: **Hardware utilization of astrocyte models**

Resource	Liu et.al [12]	Astrocyte Model-I	Astrocyte Model-II	% Decrease w.r.t [12]	
				Model-I	Model-II
Slice	3552	3463	25	2.5056	99.2962
Slice Reg	11666	231	32	98.0199	99.7257
LUTs	11394	11318	97	0.667	99.1487
BRAM	5	0	0	100	100
DSPs	42	42	4	0	90.4762

hardware-limited devices. Other hardware components (not shown in the paper) such as synapses, neurons and the input spike generators, do not contribute much to the hardware overhead.

VI. Conclusion

In this paper, a resource-efficient hardware architecture for an astrocyte-neuron self-repairing unit on an FPGA is presented. The present study helps to understand the main advantages of using hardware such as FPGAs for rapid prototyping and exploitation of inherent parallelism in brain-like self-repair mechanisms. Understanding the crucial features and extracting the required parameters are essential for mimicking the brain-like features for large scale designs. This implementation provides a stable PR at a faster instance over the prior art [8]. The results of FPGA implementations were in agreement with those of MATLAB simulations presented in [8].

VII. Acknowledgements

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References

[1] T. Horita, T. Murata, and I. Takanami, "A Multiple-Weight-and-Neuron-Fault Tolerant Digital Multilayer Neural Network," in *2006 21st IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*. IEEE, 2006, pp. 554–562.

[2] W. Barker, D. M. Halliday, Y. Thoma, E. Sanchez, G. Tempesti, and A. M. Tyrrell, "Fault Tolerance using Dynamic Reconfiguration on the POEtic Tissue," *IEEE Transactions on Evolutionary Computation*, vol. 11, no. 5, pp. 666–684, 2007.

[3] K. Reick, P. N. Sanda, S. Swaney, J. W. Kellington, M. Mack, M. Floyd, and D. Henderson, "Fault-Tolerant Design of the IBM Power6 Microprocessor," *IEEE micro*, vol. 28, no. 2, pp. 30–38, 2008.

[4] M. R. Boesen, D. Keymeulen, J. Madsen, T. Lu, and T. Chao, "Integration of the Reconfigurable Self-Healing eDNA Architecture in an Embedded System," in *Aerospace Conference*. IEEE, 2011, pp. 1–11.

[5] A. Jimenez-Fernandez, G. Jimenez-Moreno, A. Linares-Barranco, M. J. Dominguez-Morales, R. Paz-Vicente, and A. Civit-Balcells, "A Neuro-Inspired Spike-Based PID Motor Controller for Multi-Motor Robots with Low Cost FPGAs," *Sensors*, vol. 12, no. 4, pp. 3831–3856, 2012.

[6] J. A. Walker, M. A. Trefzer, S. J. Bale, and A. M. Tyrrell, "PAnDA: A Reconfigurable Architecture that Adapts to Physical Substrate Variations," *IEEE Transactions on Computers*, vol. 62, no. 8, pp. 1584–1596, 2013.

[7] M. McElholm, J. Harkin, L. McDaid, and S. Carrillo, "Bio-Inspired Online Fault Detection in NoC Interconnect," in *Energy-Efficient Fault-Tolerant Systems*. Springer, 2014, pp. 241–267.

[8] J. Wade, L. mcDaid, J. Harkin, V. Crunelli, and S. kelso, "Self-Repair in a Bidirectionally Coupled Astrocyte-Neuron (AN) System based on Retrograde Signaling," *Frontiers in Computational Neuroscience*, vol. 6, p. 76, September 2012.

[9] A. Araque, V. Parpura, R. P. Sanzgiri, and P. G. Haydon, "Tripartite Synapses: Glia, the Unacknowledged Partner," *Trends in Neurosciences*, vol. 22, pp. 208–215, June 2006.

[10] C. Edwards, "Growing Pains for Deep Learning," *Communications of the ACM*, vol. 58, no. 7, pp. 14–16, July 2015.

[11] K. Ovtcharov, O. Ruwase, J.-Y. Kim, J. Fowers, K. Strauss, and E. S. Chung, "Accelerating Deep Convolutional Neural Networks Using Specialized Hardware," Microsoft Research, [Online]. Available: https://www.microsoft.com/en-us/research/wp-content/uploads/2016/02/CNN20Whitepaper.pdf, February 2015.

[12] J. Liu, J. Harkin, L. McDaid, D. M. Halliday, A. M. Tyrrell, and J. Timmis, "Self-Repairing Mobile Robotic Car using Astrocyte-Neuron Networks," in *International Joint Conference on Neural Networks (IJCNN) (in press)*, July 2016.

[13] MaurizioDe Pittà, M. Goldberg, V. Volman, H. Berry, and E. Ben-Jacob, "Glutamate Regulation of Calcium and IP3 Oscillating and Pulsating Dynamics in Astrocytes," *Journal of Biological Physics*, vol. 35, no. 4, pp. 383–411, 2009.

[14] W. Gerstner and W. M. Kistler, *Spiking Neuron Models: Single Neurons, Populations, Plasticity*. Cambridge university press, 2002.

[15] *Divider Generator (v5.1)*, Xilinx Inc, [Online]. Available: http://www.xilinx.com/support/documentation /ip_documentation/div_gen/v5_1/pg151-div-gen.pdf, November 2015.

[16] J. Schemmel, D. Briiderle, A. Griibl, M. Hock, K. Meier, and S. Millner, "A Wafer-Scale Neuromorphic Hardware System for Large-Scale Neural Modeling," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*. IEEE, 2010, pp. 1947–1950.

[17] E. A. Bushong, M. E. Martone, Y. Z. Jones, and M. H. Ellisman, "Protoplasmic Astrocytes in CA1 Stratum Radiatum Occupy Separate Anatomical Domains," *The Journal of neuroscience*, vol. 22, no. 1, pp. 183–192, 2002.

[18] M. M. Halassa, T. Fellin, H. Takano, J.-H. Dong, and P. G. Haydon, "Synaptic Islands Defined by the Territory of a Single Astrocyte," *The Journal of neuroscience*, vol. 27, no. 24, pp. 6473–6477, 2007.

[19] E. R. Kandel, J. H. Schwartz, and T. M. Jessell, *Principles of Neural Science*, 5th ed. McGraw-Hill, November 2012.

[20] M. V. Sofroniew and H. V. Vinters, "Astrocytes: Biology and Pathology," *Acta neuropathologica*, vol. 119, no. 1, pp. 7–35, 2010.